

Intel® Ethernet Converged Network Adapter X710-DA2/DA4



Dual and Quad-port 10GbE adapters with Hardware Optimization and Offloads for the Rapid Provisioning of Networks in an Agile Data Center

Key Features

- PCI Express (PCIe) 3.0, x8
- Network Virtualization offloads including VxLAN, GENEVE, NVGRE, MPLS, and VxLAN-GPE with Network Service Headers (NSH)
- Intel® Ethernet Flow Director for hardware based application traffic steering
- Dynamic Device Personalization (DDP) enables increased packet processing efficiency for NFV and Cloud deployments
- Data Plane Development Kit (DPDK) optimized for efficient packet processing
- Excellent small packet performance for network appliances and Network Functions Virtualization (NFV)
- Intelligent offloads to enable high performance on servers with Intel® Xeon® processors
- I/O virtualization innovations for maximum performance in a virtualized server

Overview

The Intel® Ethernet Converged Network Adapter X710 addresses the demanding needs of an agile data center by providing unmatched features for both server and network virtualization, flexibility for LAN and SAN networks, and proven, reliable performance.

The Intel® Ethernet 700 Series Network Adapters. These adapters are the foundation for server connectivity, providing broad interoperability, critical performance optimizations, and increased agility for Communications, Cloud, and Enterprise IT network solutions.

- Interoperability Multiple speeds and media types for broad compatibility backed by extensive testing and validation.
- **Optimization** Intelligent offloads and accelerators to unlock network performance in servers with Intel® Xeon® processors.
- Agility Both Kernel and Data Plane Development Kit (DPDK) drivers for scalable packet processing.

Intel® Ethernet 700 Series delivers networking performance across a wide range of network port speeds through intelligent offloads, sophisticated packet processing, and quality open source drivers.

All Intel® Ethernet 700 Series Network Adapters include these feature-rich technologies:

Flexible and Scalable I/O for Virtualized Infrastructures

Intel® Virtualization Technology (Intel® VT), delivers outstanding I/O performance in virtualized server environments.

I/O bottlenecks are reduced through intelligent offloads, enabling near-native performance and VM scalability. These offloads include Virtual Machine Device Queues (VMDq) and Flexible Port Partitioning using SR-IOV with a common Virtual Function driver for networking traffic per Virtual Machine (VM). Host-based features supported include:

VMDQ for Emulated Path: VMDQ, enables a hypervisor to represent a single network port as multiple network ports that can be assigned to the individual VMs. Traffic handling is offloaded to the network controller, delivering the benefits of port partitioning with little to no administrative overhead by the IT staff.

SR-IOV for Direct Assignment: Adapter-based isolation and switching for various virtual station instances enables optimal CPU usage in virtualized environments.

- Up to 128 virtual functions (VFs), each VF can support a unique and separate data path for I/O related functions within the PCI Express hierarchy.
- Use of SR-IOV with a networking device, for example, allows the bandwidth of a single port (function) to be partitioned into smaller slices that can be allocated to specific VMs or guests, via a standard interface.

Intel® Ethernet Adaptive Virtual Function (Intel® Ethernet AVF): Customers deploying mass-scale VMs or containers for their network infrastructure now have a common VF driver. This driver eases SR-IOV hardware upgrades or changes, preserves base-mode functionality in hardware and software, and supports an advanced set of features in the Intel® Ethernet 700 Series.

Enhanced Network Virtualization Overlays (NVO)

Network virtualization has changed the way networking is done in the data center, delivering accelerations across a wide range of tunneling methods.

VxLAN, GENEVE, NVGRE, MPLS, and VxLAN-GPE with NSH Offloads: These stateless offloads preserve application performance for overlay networks, and the network traffic can be distributed across CPU cores, increasing network throughput.

Flexible Port Partitioning (FPP)

FPP leverages the PCI-SIG SR-IOV specification. Virtual controllers can be used by the Linux host directly and/ or assigned to virtual machines.

- Assign up to 63 Linux host processes or virtual machines per port to virtual functions.
- Control the partitioning of per-port bandwidth across multiple dedicated network resources, ensuring balanced QoS by giving each assigned virtual controller equal access to the port's bandwidth.

Network administrators can also rate limit each of these services to control how much of the pipe is available to each process.

Greater Intelligence and Performance for NFV and Cloud deployments

Dynamic Device Personalization (DDP) customizable packet filtering, along with enhanced Data Plane Development Kit (DPDK), support advanced packet forwarding and highly-efficient packet processing for both Cloud and Network Functions Virtualization (NFV) workloads.

- DDP enables workload-specific optimizations, using
 the programmable packet-processing pipeline.
 Additional protocols can be added to the default set
 to improve packet processing efficiency that results
 in higher throughput and reduced latency. New
 protocols can be added or modified on-demand and
 applied at runtime using Software Defined Firmware
 or APIs, eliminating the need to reset or reboot the
 server. This not only keeps the server and VMs up,
 running, and computing, it also increases
 performance for Virtual Network Functions (VNFs)
 that process network traffic that is not included in the
 default firmware. <u>Download DDP Profiles</u>
- DPDK provides a programming framework for Intel® processors and enables faster development of high-speed data packet networking applications.

Advanced Traffic Steering

Intel® Ethernet Flow Director (Intel® Ethernet FD) is an advanced traffic steering capability. Large numbers of flow affinity filters direct receive packets by their flows to queues for classification, load balancing, and matching between flows and CPU cores.

Steering traffic into specific queues can eliminate context switching required within the CPU. As a result, Intel® Ethernet FD significantly increases the number of transactions per second and reduces latency for cloud applications like memcached.

| SPET Connectivity **X710 adapters with SPF* connections support 1008ASE-SR, 1008ASE-LR and SPFP Direct Attach Copper (DAC) physical irredu. **Low-Profile from-compliance** **Inter dues office a 4ct 10 SFF*, low profile, non-PCT compliant version of the Intel** Ethernet Congregate Network Adapter XT-10-AM FF Interference of the Intel** Ethernet Congregate Network Adapter XT-10-AM FF Interference in Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** Congregate Network Adapter XT-10-AM FF Intel** and Intel** Adapter XT-10-AM FF Intel** Adapter XT-10-AM F | FEATURES | DESCRIPTION |
|--|--|---|
| physical models. Deveronible from-compilance) Intel discos offer a Act O SFP I, low profile, non-PCI compilant vention of the Intel® Ethernet Converged Network Adaptor X710-DAP II. Please contact your Intel representative for information about this adaptor. Full-Height Intel® Self-Memor Converged Network Adaptor X710-DAP AFF requires a full highly stor for PCI compilance. Intel® Self-Memor Converged Network Adaptor X710-DAP AFF requires a full highly stor for PCI compilance used with Receive-Size Self-Memor Adaptor X710-DAP AFF requires a full highly stor for PCI compilance. Full-Height The Intel Ethernet 700 Series implements a design philosophy of platform resiliency with a stributes series the New York Self-Memor Adaptor X710-DAP AFF requires at stributes verify the Remarca and critical device settings with thousit in corruption detection and automated device receivery to return the device to strongly programmed of adaptic settings with the European Turnor adaptication. Support for most network operating systems Enables broad deligion/ment for different applications. Time Sync (IEEE 1588, 802.1ag) Enables broad deligion/ment for different applications. Finel Sync (IEEE 1588, 802.1ag) Enables retworked themere equipment to synchronize internal clocks according to a network master clock endoption can then anguire an accurate estimate of the master time by compensating for link latency. **Violent Ethernet Sync Director (Intel® 1588, 802.1ag) Intel® Ethernet Size Director (Intel® 1588, 802.1ag) Envir Ethernet Size Director (Inte | General | |
| Adaptive 7710-04 PH. Please contact, your Intel representative for information about this adaptive. Full-Height Intel® Hithment Converged Newton-Adaptive 77.00-04 PH requirse a fluid pelly set for EPG compliance. Increases performance on multi-processor systems by efficiently balancing network loads a cross CPU core when used with Receives-Side English (RSS) from Microards or scalable (IQ on Linux.) Protect, Detect and Recover The Intel Ethment 700 Series implements a design pilloloopy of platform residiency with 1 attributes supporting the NIST Cybenecurity Transcore. Protect, Detect and Recover. The statistics everying the Charles of the NIST Cybenecurity Transcore. Protect, Detect and Recover. The statistics everying the Charles of the NIST Cybenecurity Transcore. Protect, Detect and Recover. The statistics of the NIST Cybenecurity Transcore. Protect, Detect and Recover. The statistics of the NIST Cybenecurity Transcore and automated device recovery to return the device to a solidary programmed statistic. Support for must network operating systems Complete with the European Union directive 2011/89/EU to reduce the use of hazardous materials. Time Sync (IEEE 1988, 802.1a) Enables networked between equipment to synchronize internal clocks according to a network master clock endoor can then acquire an accurate estimate of the master time by compensating for link latency. I/O Features for Multi-Core Processor Servers Intel® 15th Transcore (Intel® 15th Transcore) (Intel® 15th Tran | SFP+ Connectivity | |
| Increases, per formance on multiple CPUs Increases, per formance on multiple cores, of the centry balancing person loads accass CPU care when used with Receive*-Sellagi (RSS) from cort of scalable (FO on Linux.) | Low-Profile (non-compliance) | , , , , |
| used with Receive-Side Scaling (RSS) from Microsoft or scalable (PO on Linux. 1. The lite Etheries (200 points implements a design philosopoly of pathorn reallency with 3 attributes supporting the INST Cybersecurity Framework: Protect, Detect and Recover. These attributes wrifty the firmware and critical device settings with build-in corruption detection and automated device recovery to return the device to its originally programmed state. Simport for most network operating systems RoHS-compliant 1. Complies with the European Union directive 2011/6/5/EU to reduce the use of hazardous markers in the system of the European Union directive 2011/6/5/EU to reduce the use of hazardous markers. 1. Complies with the European Union directive 2011/6/5/EU to reduce the use of hazardous markers clock endpoint can then acquire an accurate estimate of the master time by complemating for link latency. 1. Vo Features for Multi-Core Processor Servers 1. Comerce Time 1. Advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud applications like Memcached. 1. Milligate Consume 1,336 Ts and Ric queues 1. Milligate Consume 1,336 Ts and Ric queues 1. Explored Time 1. Advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud applications like Memcached. 1. Milligate Consume 1,336 Ts and Ric queues 1. Milligate Consume 1,336 Ts and Ric queues 1. Explored Time 1. Advanced Processor Servers 1. Advanced Packet processor stage of interrupts. 1. Load-balancing of interrupts. 1. | Full-Height | • Intel® Ethernet Converged Network Adapter X710-DA4 FH requires a full height slot for PCIe compliance. |
| the NIST Cybersecurity Framework: Protect, Detect, and Recover. These attributes verify the firmware and critical device settings with built-in corruption detection and submated device recovery to return the device to his originally programmed state. Support for most network operating systems - Embles broad deployment for different applications. RoH5-compliant - Compliant - Compliant - Compliant Security of the Compliant Security of Security | Load balancing on multiple CPUs | |
| ReHS-compliant Complies with the European Union directive 2011/05/EU to reduce the use of hazardous materials. Fine Sync (IEEE 1588, 902 lass) -Enables networked Ethernet to synchronize internal clocks according to a network material cody endoptic and the material and cody according to a network material cody. Possible for Multi-Core Processor Servers Intel® 15thernet Flow Director - An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud applications like Memcached. - Mish Support - Minimizes the overflow of multiple cores/CPUs. Multiple Queues 1,536 Ts and Rx queues - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing efficient packet prioritization. - Network packet handling without waiting for buffer overflow providing place to the waiting packet buffer in the hypervisor of the hypervisor packet place without packet type. Virtualization Features Nett-generation VMDq - Up to 256 maximum VMDq VMs supported. - Officias the data-socing based on MAC addresses and VLAN tags, functionality from the Hypervisor to the networks illicon, improving data throughput and CPU usage. PCI-SIG SR-IOV implementation - Up to 256 disasting before the provides an implementation of the PCI-SIG standard for I/Q Virtualization. The physical configuration of each port is divided into multiple virtual ports. - Vir | Protect, Detect and Recover | the NIST Cybersecurity Framework: Protect, Detect and Recover. These attributes verify the firmware and critical device settings with built-in corruption detection and automated device recovery to return the device to |
| Enables networked Ethernet equipment to pyrichronize internal clocks according to a network matter clock endpoint can then acquire an accurate estimate of the master time by compensating for link latency. ### Chement Flow Director (insel* Ethernet Flow Director (insel* Ethernet Flow Director (insel* Ethernet Flow Director) ### An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud applications like Memcached. ### MIST'S support **An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud splications like Memcached. #### MIST'S support **An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud splications like Memcached. #### MIST'S support **An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud splications like Memcached. #### MIST'S support **An advanced traffic steering capability increases the number of transactions per second and reduces latency for cloud splications like Memcached. **Actual number of queues will vary depending upon software implementation. **Actual number of queues will vary depending upon software implementation. **Actual number of queues will vary depending upon software implementation. **Actual number of queues will vary depending upon software implementation. **Checksum and segmentation capability extended to new standard packet type. **VITALE 300 (Provides traffic and MAC addresses and VLAN tags, functionality from the Hypervisor to the network silication improving data throughput and CPU Just's subject of the PCLSIG standard for (VIO Virtualization. The physical configuration of each port (128 per device) **Provides an implementation of the PCLSIG standard for (VIO Virtualization. The physical configuration of each port virtual six his provided that provides traffic load balancing (Tx and Rx) across VMs bound to the team | Support for most network operating systems | Enables broad deployment for different applications. |
| endpoint can then acquire an accurate estimate of the master time by compensating for link latency. ### Fiber ### Flow Director Intel® Fiber ### Flow Dire | RoHS-compliant | • Complies with the European Union directive 2011/65/EU to reduce the use of hazardous materials. |
| Intel® Ethernet Flow Director (Intel® Ethernet Flow Director) (Inte | Time Sync (IEEE 1588, 802.1as) | |
| (Intel® Ethernet FD) cloud applications like Memicached. MSI-X support Militripies to vereinhead of interrupts Load-balancing of interrupt handling between multiple cores/CPUs Modern Park device - Park device - Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing for buffer overflow providing efficient packet prioritization Actual number of queues without valuing possible values of the packet for the packet prioritization Actual number of queues without values of the packet to provide a minimum value provided to new standard packet type. Virtualization Features Next-generation VMDq - Up to 256 maximum VMDq VMs supported Up to 256 maximum VMDq VMs supported Officials the data-sorting based on MAC addresses and VLAN tags, functionality from the Hypervisor for the network silicon, improving data throughput and CPU usage Provides an implementation of the PCLSIG standard for I/O Virtualization. The physical configuration of each port is divided into multiple virtual ports. Each virtual port is assigned to an individual VM directly by bypassing the virtual standard packet prioritized addresses in the memory to each VMs 6/6/port for dual port. Virtual Machine Load Balancing (VLMB) - VMLB provides a further layer port portion standard packet prioritized for prioritization in the tevent of switch, port, cable, or adapter failure. Advanced Packet Filtering - 15/26 exact matched packets (pincient VT-G1) to provide data protection between VMs 6/6/port for fuice VT-G1 to provide data pro | I/O Features for Multi-Core Processor S | Servers |
| Load-balancing of interrupt handling between multiple cores/CPUs. Multiple Queues: 1,536 Tx and Rx queues Network packet handling without waiting for buffer overflow providing efficient packet prioritization. | | |
| PCI-SIG SR-IOV Implementation 1. Virtualization Features Next-generation VMDq 1. Up to 256 maximum VMDq VMs supported. 2. Officiads the data-sorting based on MAC addresses and VLAN tags, functionality from the Hypervisor to the network silicon, improving data throughput and CPU usage. PCI-SIG SR-IOV Implementation (128 per device) PCI-SIG SR-IOV Implementation (128 per device) PCI-SIG SR-IOV Implementation (128 per device) Provides an implementation of the PCI-SIG standard for I/O Virtualization. The physical configuration of each port is divided into multiple virtual ports. Each virtual ports assigned to an individual VM directly by bypassing the virtual winth in the Hypervisor, resulting in mean-native performs. PVI-UP to Directed I/O (Intel* VT-Id) to provide data protection between VMs by assigning separate physical addresses in the memory to each VM. PVI-UP to Virtual Machine Load Balancing (VLMB) Virtual Machine Load Balancing (VLMB) Virtual Machine Load Balancing (VLMB) VIVILLIA INTERVITED AND ADDRESS A | MSI-X support | |
| Checksum and segmentation capability extended to new standard packet type. | | |
| Next-generation VMDq - Up to 256 maximum VMDq VMs supported Officads the data-sorting based on MAC addresses and VLAN tags, functionality from the Hypervisor to the network silicon, improving data throughput and CPU usage. PCI-SIG SR-IOV implementation (128 per device) - Provides an implementation of the PCI-SIG standard for I/O Virtualization. The physical configuration of each port is divided into multiple virtual ports. Each virtual port is assigned to an individual VM directly by bypassing the virtual way in the Hypervisor, resulting in near-native performance Integrated with Intel* VIT for Directed I/O (Intel* VT-d) to provide data protection between VMs by assigning separate physical addresses in the memory to each VM 84/port for dual port. Virtual Machine Load Balancing (VLMB) - VMLB provides traffic load balancing (Tx and Rx) across VMs bound to the team interface, as well as fault tolerance in the event of switch, port, cable, or adapter failure. Advanced Packet Filtering - VLAN support with VLAN tag insertion, stripping and packet support and multicast Diversional Stripping and packet support and multicast Diversional Stripping of Invalid frames. VLAN, NVGRE, GENEVE, VxLAN-GPE+NSH, MPLS - Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support - Enables system boot via the LAN (32-bit and 64-bit) Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) - Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware Easy system monitoring with industry-standard consoles. SPECIFICATIONS General - Omnections - Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers - Network Standard Physical Layer Interfaces | | · |
| Officials the data-sorting based on MAC addresses and VLAN tags, functionality from the Hypervisor to the network silicon, improving data throughput and CPU usage. PCI-SIG SR-IOV Implementation (128 per device) Provides an implementation of the PCI-SIG standard for I/O Virtualization. The physical configuration of each port is divided into multiple virtual ports. Each virtual port is assigned to an individual VM directly by bypassing the virtual within the Hypervisor, resulting in near-native performance. Integrated with Intel® VT for Directed I/O (Intel® VT-d) to provide data protection between VMs by assigning separated physical addresses in the memory to each VM. 64/port for dual port. Virtual Machine Load Balancing (VLMB) VMLB provides traffic load balancing (Tx and Rx) across VMs bound to the team interface, as well as fault tolerance in the event of switch, port, cable, or adapter failure. Advanced Packet Filtering 1536 exact matched packets (unicast or multicast). 1512 hash entries each for unicast and multicast). 1512 hash entries each for unicast and multicast. 1500 to 4096 VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags VXLAN, NVGRE, GENEVE, VXLAN-GPE+NSH, MPLS Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support 1512 hash entries each for up to 4096 VLAN tags Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support 1512 hash entries each for PXE image. 1513 hash entries each for pXE image. 1514 hash entries each for pXE image. 1515 hash entries each for pXE image. 1516 hash entries each for pXE image. 1517 hash entries each for pXE image. 1518 hash entries each for pXE image. 1518 historicast and multicast) transfer mode support. 1518 historicast and multicast) transfer mode support. 1519 hash entries each for unicast and multicast) transfer mode support. 1510 hash entries each fo | Virtualization Features | |
| is divided into multiple virtual ports. Each virtual ports assigned to an individual VM directly by bypassing the virtual switch in the Hypervisor, resulting in near-native performance. Integrated with Intel® VT for Directed I/O (Intel® VT-d) to provide data protection between VMs by assigning separate physical addresses in the memory to each VM. Virtual Machine Load Balancing (VLMB) VMLB provides traffic load balancing (Tx and Rx) across VMs bound to the team interface, as well as fault tolerance in the event of switch, port, cable, or adapter failure. Advanced Packet Filtering 1536 exact matched packets (unicast or multicast). 1512 hash entries each for unicast and multicast). 1512 hash entries each for unicast and multicast. 10-wer processor usage. Promiscuous (unicast and multicast) transfer mode support. Optional filtering of invalid frames. VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags VLAN, NVGRE, GENEVE, VXLAN-GPENSH, MPLS Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support Enables system boot via the LAN (32-bit and 64-bit). Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. Easy system monitoring with industry-standard consoles. Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters **Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. **SPECIFICATIONS** General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers | Next-generation VMDq | Offloads the data-sorting based on MAC addresses and VLAN tags, functionality from the Hypervisor to the |
| Virtual Machine Load Balancing (VLMB) • VMLB provides traffic load balancing (Tx and Rx) across VMs bound to the team interface, as well as fault tolerance in the event of switch, port, cable, or adapter failure. • 1536 exact matched packets (unicast or multicast). • 512 hash entries each for unicast and multicast. • Lower processor usage. • Promiscuous (unicast and multicast) transfer mode support. • Optional filtering of invalid frames. VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags VXLAN, NVGRE, GENEVE, VXLAN-GPE+NSH, MPLS • Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support • Enables system boot via the LAN (32-bit and 64-bit). • Flash interface for PXE image. • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. • Easy system monitoring with industry-standard consoles. • Easy system monitoring with industry-standard consoles. • Event of preserves and indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. • SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces | · · · · · · · · · · · · · · · · · · · | is divided into multiple virtual ports. Each virtual port is assigned to an individual VM directly by bypassing the virtual switch in the Hypervisor, resulting in near-native performance. Integrated with Intel® VT for Directed I/O (Intel® VT-d) to provide data protection between VMs by assigning separate physical addresses in the memory to each VM. |
| | Virtual Machine Load Balancing (VLMB) | |
| packet filtering for up to 4096 VLAN tags VxLAN, NVGRE, GENEVE, VxLAN-GPE+NSH, MPLS Preserves application performance in network virtualized environments. Manageability Features Preboot Execution Environment (PXE) Support • Enables system boot via the LAN (32-bit and 64-bit). • Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters Watchdog Timer • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | Advanced Packet Filtering | 512 hash entries each for unicast and multicast. Lower processor usage. Promiscuous (unicast and multicast) transfer mode support. |
| Manageability Features Preboot Execution Environment (PXE) Support • Enables system boot via the LAN (32-bit and 64-bit). • Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | | Ability to create multiple VLAN segments. |
| Preboot Execution Environment (PXE) Support • Enables system boot via the LAN (32-bit and 64-bit). • Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | VxLAN, NVGRE, GENEVE, VxLAN-GPE+NSH, MPLS | Preserves application performance in network virtualized environments. |
| • Flash interface for PXE image. Unified Extensible Firmware Interface (UEFI) • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters Watchdog Timer • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | Manageability Features | |
| Simple Network Management Protocol (SNMP) and Remote Network Monitoring (RMON) Statistic Counters Watchdog Timer • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | Preboot Execution Environment (PXE) Support | |
| Remote Network Monitoring (RMON) Statistic Counters Watchdog Timer • Gives an indication to the manageability firmware or external devices that the controller or the software device driver is not functioning. SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | Unified Extensible Firmware Interface (UEFI) | • Enables new technologies during the pre-OS boot process and addresses legacy BIOS limitations on hardware. |
| SPECIFICATIONS General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | | |
| General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | Watchdog Timer | |
| General Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | SPECIFICATIONS | |
| Connections Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | | |
| Network Standard Physical Layer Interfaces 10GBASE-SR and -LR optical transceivers | | Dual or Quad SFP+ cages supporting Direct Attach Copper (DAC) Twinaxial cable and optical transceivers |
| | | |

| Technical Features | | |
|-----------------------|---|--|
| Operating Temperature | 0 °C to 55 °C (32 °F to 131 °F) | |
| Airflow | 150 LFM with 55 °C required for CR (DAC) 150 LFM with 55 °C or 500 LFM with 65 °C required with extended temp SR optics | |
| Storage Temperature | -40 °C to 70 °C (-40 °F to 158 °F) | |
| Storage Humidity | Maximum: 90% non-condensing relative humidity at 35 °C | |
| LED Indicators | LINK (solid) and ACTIVITY (blinking) LINK SPEED (green = 10Gbps; yellow = 1Gbps) | |

| Adapter Features | |
|------------------------------|---------------------------------------|
| Data Rate Supported Per Port | Optical: 1/10GbE Direct Attach: 10GbE |
| Bus Type | PCIe 3.0 (8 GT/s) |
| Bus Width | PCIe x8 |
| Interrupt Levels | INTA, MSI, MSI-X |
| Hardware Certifications | FCC A, UL, CE, VCCI, BSMI, CTICK, KCC |
| Controller | Intel® Ethernet Controller X710-BM2 |

| Power Consumption | | | | |
|----------------------------------|---------------|---------------|--|--|
| SKU | Typical Power | Maximum Power | | |
| Dual-port 10GBASE-SR | 4.3 W | 4.8 W | | |
| Dual-port 1000GBASE-SX | 4.0 W | 4.3 W | | |
| Dual-port 10GBASE-LR | 4.5 W | 5.1 W | | |
| Dual-port Direct Attach (Twinax) | 3.3 W | 3.7 W | | |
| Quad-port 10GBASE-SR | 6.2 W | 6.6 W | | |
| Quad-port 1000GBASE-SX | 5.5 W | 6.0 W | | |
| Quad-port 10GBASE-LR | 6.9 W | 7.4 W | | |
| Quad-port Direct Attach (Twinax) | 3.6 W | 3.8 W | | |

| Physical Dimensions | |
|----------------------|-----------------|
| X710-DA2 Low profile | 167 mm x 69 mm |
| X710-DA4 Full height | 167 mm x 111 mm |
| X710-DA4 Low profile | 167 mm x 69 mm |

| Product Order Code | | | | |
|--------------------|--------------|----------------|--|--|
| Configuration | Product Code | Adapter Height | | |
| Dual Port | X710DA2 | Low profile | | |
| Quad Port | X710DA4FH | Full height | | |
| Quad Port | X710DA4G2P5 | Low profile | | |

Supported Operating Systems

For a complete list of supported network operating systems for Intel® Ethernet 700 Series Adapters visit: intel.com/support/EthernetOS

Intel® Ethernet Accessories

Intel® Ethernet Optics and Cables are proven, reliable solutions for high-density Ethernet connections. Combine these accessories with Intel® Ethernet 700 Series and 500 Series Network Adapters for dependable interoperability and consistent performance across the network. Learn more at intel.com/ethernetproducts

Warranty

Intel limited lifetime hardware warranty, 90-day money-back guarantee (U.S. and Canada) and worldwide support.

Customer Support

For customer support options in North America visit: intel.com/content/www/us/en/support/contact-support.html

Product Information

For information about Intel® Ethernet Products and technologies, visit: intel.com/ethernetproducts

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

The products and services described may contain defects or errors which may cause deviations from published specifications.

© Intel Corporation. Intel, the Intel logo, Xeon, and other Intel marks are trademarks of Intel Corporation or its subsidiaries.

Other names and brands may be claimed as the property of others.



Printed in USA 0121/ED/123E

Please Recycle 🗳

331180-013US